**IN THE SPECIFICATION:**

Please insert before the first sentence on page 1 the following:

This application is a divisional application of U.S. Application No. 09/979,188, filed on November 20, 2001, which was a national stage filing under 35 U.S.C. §371 of International Application No. PCT/JP01/02171 filed on March 19, 2001.

Please replace the paragraph beginning at Page 3, line 33 and ending on Page 4, line 7, with the following:

Moreover, it is now assumed that the semiconductor chip 101b and the mounting board ~~103~~ 108 have a small gap therebetween. In this case, even if the semiconductor chip 101b does not contact the mounting board 108 when mounted, the mounting board 108 may be subjected to bending or torsional stresses by external pressure and the like generated when the product is in use. This would cause the surface of the semiconductor chip 101b to contact the mounting board 108, damaging the semiconductor chip 101b.

Please replace the paragraph beginning at Page 9, line 18 and ending on Page 10, line 10, with the following:

Fig. 1 is a cross-sectional view showing the schematic structure of a semiconductor device according to a first embodiment of the present invention; Fig. 2 is a cross-sectional view showing the schematic structure of a semiconductor device according to a fourth embodiment of the present invention; Fig. 3 is a cross-sectional view showing the schematic structure of a semiconductor device according to a fifth embodiment of the

present invention; Fig. 4 is a cross-sectional view showing the schematic structure of a semiconductor device according to the fifth embodiment of the present invention; Fig. 5 is a plan view showing the schematic structure of a semiconductor device according to the fifth embodiment of the present invention; ~~Fig. 6~~ Figs. 6A, 6B and 6C ~~is a~~ are process ~~chart~~ charts illustrating a method for manufacturing a semiconductor device according to a sixth embodiment of the present invention. Fig. 6A shows the state in which an electronic component is mounted on the top surface of a wiring substrate. Fig. 6B shows the state in which a semiconductor chip is mounted on the back surface of the wiring substrate. Fig. 6C shows the state in which projecting electrodes have been formed on the back surface of the wiring substrate; ~~Fig. 7~~ Figs. 7A, 7B and 7C ~~is a~~ are process ~~chart~~ charts illustrating a method for manufacturing an electronic equipment according to a seventh embodiment of the present invention. Fig. 7A shows the state that a conductive connecting material has been formed on electrodes of a mounting board. Fig. 7B shows the state in which a semiconductor device is mounted on the mounting board. Fig. 7C show the state in which the mounting board was heated and then cooled to room temperature; Fig. 8 is a perspective view showing the schematic structure of a portable information terminal according to an eighth embodiment of the present invention; Fig. 9 is a cross-sectional view showing the schematic structure of the portable information terminal according to the eighth embodiment of the present invention; Fig. 10 is a cross-sectional view showing the schematic structure of a portable information terminal according to a ninth embodiment of the present invention; Fig. 11 is a cross-sectional view showing the schematic structure of a conventional semiconductor device; Fig. 12 is a cross-sectional view showing the

schematic structure of a conventional semiconductor device; and Fig. 13 is a cross-sectional view showing the schematic structure of a conventional semiconductor device.

Please replace the paragraph beginning at Page 13, line 4, with the following:

Moreover, in the present embodiment, the warping was calculated with various thicknesses of the first semiconductor chip 1a, the second semiconductor chip 1b and the wiring board 3. When the thickness of the first semiconductor chip 1a is less than 0.3 mm, the rigidity is significantly reduced, whereby the warping is abruptly increased. It is therefore preferable to set the thickness of the first semiconductor chip 1a to 0.3 mm or more so as to prevent reduction in rigidity of the semiconductor device ~~1~~ 10 as a complex.

Please replace the paragraph beginning at Page 15, line 23 and ending on Page 16, line 6, with the following:

~~Fig. 6~~ Figs. 6A, 6B and 6C ~~is a~~ are process ~~chart~~ charts illustrating a method for manufacturing a semiconductor device according to the sixth embodiment of the present invention. In the present embodiment, as shown in Fig. ~~6(a)~~ 6A, connection electrodes 2 of an electronic component 1a are first aligned with respective electrodes of a wiring substrate 3. The connection electrodes 2 are melted for connection by using, e.g., a flip chip bonding method, and the gap between the electronic component 1a and the wiring substrate 3 is then filled with a sealing resin 5 in order to improve connection reliability. In the case where a substrate formed from a resin is used as the wiring substrate 3, the linear expansion coefficient thereof is about 15 to 40 x $10^{-6}$ (1/°C), which is larger than

about 3 to 6 x $10^{-6}$ (1/°C) of the electronic component 1a formed from a semiconductor such as silicon and gallium arsenide. Accordingly, when the electronic component 1a is connected onto the wiring substrate 3 in a heated state and then cooled to room temperature, the wiring substrate 3 is shrunk more than the electronic component 1a. Therefore, at this time, the wiring substrate 3 is warped so as to project toward the electronic component 1a.

Please replace the paragraph beginning at Page 16, line 7, with the following:

As shown in Fig. ~~6(b)~~ 6B, connection electrodes 2 of a second semiconductor chip 1b are then aligned with respective electrodes 4 on the other surface of the wiring substrate 3, and connected therewith by heating and cooling in the same manner. Thereafter, the gap between the second semiconductor chip 1b and the wiring substrate 3 is filled with a sealing resin 5 in order to improve connection reliability. Since the second semiconductor chip 1b is thinner than the electronic component 1a and has small force to bend the wiring substrate 3, the wiring substrate 3 remains warped so as to project toward the electronic component 1a.

Please replace the paragraph beginning at Page 16, line 19 and ending on Page 20, line 2, with the following:

As shown in Fig. ~~6(c)~~ 6C, projecting electrodes 7 are then formed in the periphery of the wiring substrate 3. For example, the projecting electrodes 7 are formed by arranging solder balls 7 on the electrodes 4 of the wiring substrate 3 and melting the solder

by heating. The projecting electrodes may alternatively be formed by printing cream solder on the electrodes 4 of the wiring substrate 3 and heating it. For example, in order to arrange the solder balls at intervals of 0.5 mm, solder balls having a diameter of about 0.3 mm are used. In this case, the projecting electrodes 7 have a height of about 0.23 mm. Accordingly, provided that the projecting electrodes 7 are mounted on a mounting board (not shown) in the following conditions: the second semiconductor chip 1b has a thickness of 0.15 mm; the connection electrodes 2 for connecting the second semiconductor chip 1b to the wiring substrate 3 have a height of 30 $\mu$m; the electrodes 4 on the wiring substrate 3 have a thickness of 20 $\mu$m; and the warping amount of the wiring substrate is 10 $\mu$m, spacing of about 30 $\mu$m can be assured between the second semiconductor chip 1b and the mounting board even if the warping is recovered by 10 $\mu$m when mounted on the mounting board.

Please replace the paragraph beginning at Page 17, line 17, with the following:

Alternatively, flip chip bonding using solder may be employed. An alloy such as lead tin or silver tin is used as solder, and the solder can be formed by, e.g., vapor deposition, printing of solder paste, ball bonder and the like. Instead of the solder, a material such as gold and copper may be used. In this case, connection can be realized with a conductive adhesive or conductive particles interposed between the connection electrodes 2 and the electrodes ~~4~~ 2 of the wiring substrate 3. Alternatively, connection may be realized with solder interposed between the connection electrodes 2 and the

electrodes 4 of the wiring substrate 3. Instead of the flip chip bonding, wire bonding may be used.

Please replace the paragraph beginning at Page 18, line 2, with the following:

~~Fig, 7~~ Figs. 7A, 7B and 7C ~~is a~~ are process ~~chart~~ charts illustrating a method for manufacturing an electronic equipment according to the seventh embodiment of the present invention. In the present embodiment, as shown in Fig. ~~7(a)~~ 7A, a conductive connecting material 16 is formed on electrodes 9 of a mounting board 8. For example, the conductive connecting material 16 is a cream-like material of fine solder particles dissolved in a solvent, and is formed by printing. The height of the conductive connecting material ~~10~~ 16 depends on the spacing between the electrodes, and is about 0.1 mm when the spacing between the electrodes is 0.5 mm.

Please replace the paragraph beginning at Page 18, line 11, with the following:

Fig. ~~7(b)~~ 7B shows the state in which a semiconductor device 10 is mounted on the mounting board 8 after the electrodes 9 on the mounting board 8 are aligned with projecting electrodes 7 of the semiconductor device ~~16~~ 10 (no heating was conducted). The warping amount of the wiring substrate 3 is herein within 100 $\mu$m so that the projecting electrodes 7 of the semiconductor device 10 sufficiently contact the conductive connecting material ~~10~~ 16.

Please replace the paragraph beginning at Page 18, line 18, with the following:

Fig. ~~7(c)~~ 7C shows the state in which the mounting board was heated at about 240°C to melt the solder, and then cooled to room temperature. When a glass epoxy resin containing glass fiber is used as the mounting board, the mounting board has a smaller linear expansion coefficient than the wiring substrate 3 formed from a resin material or a composite material containing a resin material at a high ratio. Therefore, thermal contraction of the mounting board is smaller than the wiring substrate, so that warping of the wiring substrate 3 is reduced as compared to the state of Fig. ~~7(b)~~ 7B.

Please replace the paragraph beginning at Page 18, line 26, with the following:

In the present embodiment, the warping amount reduced in the state of Fig. ~~7(c)~~ 7C from the state of Fig. ~~7(b)~~ 7B was about 10 $\mu$m. Accordingly, the spacing of several tens of micrometers was able to be assured between the second semiconductor chip 1b and the mounting board 8.